A REVIEW OF FLIP-FLOP DESIGNS FOR LOW POWER VLSI CIRCUITS

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ABSTRACT
Flip-flop topologies are highly effective in the development of VLSI in-built circuits. These circuits are actually high performing CMOS circuits that can give a marvelous speed to the system. At the same time, it is necessary to choose the right flip-flop for a given application to get the desired design to satisfy the need of high performing circuit that would consume low power. In this paper, we will come across various types of flip-flops with a wide array of topologies that vary are specifications in terms of area estimation, power dissipation estimation, transistor count, simulation set up, etc. In this context, the concept of optimum design is also discussed. The work pattern of every flip-flop is explained properly and simulation is made with “micro wind” and LT-SPICE. The analysis of these flip-flops is made with respect to the parameters like propagation delays at 0.12μm 6metal coating technology and power dissipation is carried out.

Keywords: VLSI, High speed, flip-flops, power dissipation, topologies

INTRODUCTION
In the very large scale integrated circuits or VLSI circuits, a wide array of sequential circuits like counters, registers, memory elements, are used. With the improvement in the VLSI technology, the integration level is getting better and the clock speed is also enhancing with time. For the improved design of CSE (Clock Storage Element) that will provide high speed but will consume low energy submicron, topology selection, and CMOS system area are too important. Portable batteries and microprocessors that have been in wide demand these days are the best examples of today’s improved design of CSE.

Different categories of flip-flops are available these days that can produce high speed at lower energy consumption levels. Getting hand into the most appropriate flip-flop topology suitable for a specific application is not an easy affair as you can find a large number of different types of topology meeting your need. In any case, a prominent design and the best possible topology are required to achieve the desired result from a CMOS circuit.

Being a bi-stable circuit, a flip-flop is capable of storing a logic state either 0 or 1 in response to the pulse emanated from the clock. In the design of the digital circuit, a large part of the design is engaged in the synchronization which operates on the basis of the signal produced the clock. It remarkably
reduces the complexity of the circuit design. In this respect, the key challenge lies in the design of an affable D flip-flop (DFF).

The evaluation of different types of topology can be started with flip-flop set that is triggered with a conventional single edge. This normally fixes the data either at the negative or positive end of the attached clock. A SET FF is organized to function as a master-slave latch by flowing the successive structure. This process is incompetent because in this system one part of the clock edges are lost but the complete application expense is incurred for the clock.

Next, we are concerned about flip-flop DET gets active through Double Edge trigger. The benefit of this flip-flop is that it can be triggered both positive and negative edges. Several types of topologies are proposed in this context but these specifications are not so efficient as they bring compact driving capabilities that cause DC power consumption at the output node. The topology presented in this study is drawn with an aim to overcome the barriers of the previous drawbacks. The third topology used in this context to describe the semi-dynamic flip-flop with both dynamic and static designs is described in [1]. The best aspect of this flip-flop is that it can provide both short latency and prepare relevant logic functions with the least delay time. These characteristics are essential for the formation of high-performance microprocessors. A discussion is made on HLFF or Hybrid Latch Flip-Flop. HLFF is made to lessen the latch and the load on the clock simultaneously [2].

Pulsed-Triggered Flip-Flop P-FF is the next most important topology. It possesses strobe signals and a latch for data storage. These kinds of flip-flops are perfect for all those applications where high-speed is necessary and where clock sensitivity is low. Discussion on SAFF or Sense-Amplifier-Based Flip-Flop is also made in [3] that makes real and complementary inputs and also suitable for producing real complementary outputs.

Another discussion is made on sense-amplifier-based FF. It's visible drawback called the slave element is consisted of Set/Reset (SR) NAND latches that suffer from the chance of that the inner nodes will float at the minimum level if the inputs switch to 0 or 1 when the level of the clock is high [4] [5]. At the same time, these kinds of transistors require the minimum possible number of transistors which provides asymmetrical interruptions that can be called clock-to-output delay that fluctuates from the high-to-low output. Our discussion on STFF has eliminated these sorts of issues to a great extent. In different features of WPMS or Write Port Master Slave FF are described that possesses the structure apart from pMOS in the concerned pass gate [6]. The framework of WPMS may be called “inverter-pass transistor” which is a combination that decouples the available data path with the inverters used for the clock. The net result is smooth-sailing dispersal of the available gain which is also responsible for accepting lower energy helping the best possible designs.

A detailed explanation is made for TSPC or True Single Phased clacking. This is a proven process to obtain quick VLSI design. TSPC is a much-protected process that requires minimum routing area for the clock signal [7]. On the other hand, discussion is made on a positive edge trigger register that is created on the master-slave idea that is not at all sensitive to any overlap of clock known as clocked CMOS or C²MOS [8]. A vast discussion will be visible in the area of power dissipation area estimation as also on comparison strategy and innovative analysis. The purpose of the comparison strategy is to compare a large array of flip-flop topology in 0.12μm CMOS technology [9].

POWER CONSUMPTION IN STORAGE ELEMENT

Designers have been facing a critical problem in the management of power consumption process in the integrated high-performance circuits. Most obvious sources of power dissipation in the latch are as follows:

1. Local data power dissipation: It presents that part of the power dissipated in the logical stage of the data processing.

2. Internal power dissipation: It represents the power required to switch the output load.
Local clock power dissipation: It represents that part of the power dissipated in the buffer of the local clock that is required to drive the clock input.

The total parameter measured in this matter is the sum of all these above three aspects.

It could be observed that the digital VLSI clocking system (Fig. 1) [10]. In a circuit with proper synchronization, the power consumption $P_{cs}$ is measured in the following way:

$$P_{cs} = P_{eg} + P_{gw} + P_{lw} + P_{f} + P_{ff} = (1 + B^1 + B^2 + B^3 + ... + B^N) \cdot V_s^2 \cdot f(C_{gw} + C_{lw} + C_{fg}) + P_{ff}$$

Block diagram of a digital VLSI showing the clocking system

Source: Nedovic, Oklobdzija and Walker, 2003

Here, the clock generator is represented through $P_{eg}$, global wiring capacitance through $P_{gw}$, local wiring capacitance through $P_{lw}$, total clocked gate capacitance through $P_{fg}$, power dissipation by all the flip-flops $P_{ff}$. Again,

$\beta$ = Tapering factor of the clock generator

$N$ = Tapering stages number in the clock buffer

$V_s$ = Voltage swing of the clock distribution network

$F$ = Clock frequency

$C_j$ = here $j$ stands for junction capacitance in the region of the source-drain regions of the output node of the clock generator

$C_{gw}$ = $gw$ stands of global wires, it presents total parasitic capacitance

$C_{lw}$ = $lw$ represents local wires and the expression measures the total parasitic capacitance of it

$C_{fg}$ = $g$ stands for gate capacitance, and the expression represents the clocking system.

$P_{ff}$ = the power dissipation in all the FFs, i.e. the power dissipation due to switching output loads + local clock buffer + logic stage driving the data input

Total power dissipation in a synchronous system can be reduced by choosing the proper values of $\beta$ and reducing the values of $C_{gw}$, $C_{lw}$, $C_{fg}$, $V_s$, $f$.

ELUCIDATION OF FLIP-FLOP TOPOLOGY

As said previously, a wide array of topology is chosen in this matter, they are as follows:

1. Single Edge-Triggered Flip-Flop (SET)
2. Double Edge-Triggered Flip-Flop (DET)
3. Semi-Dynamic Flip-Flop (SDFF)
4. Hybrid Latch Flip-Flop (HLFF)
5. Pulse-Triggered Flip-Flop (P-FF)
6. Sense-Amplifier-Based Flip-Flop (SAFF)
7. Write-port Master-Slave Flip-Flop (WPMS)
8. True Single-Phase-Clock Flip-Flop (TSPC)
9. Clocked CMOS Flip-Flop (C2CMOS)

Here, we have the detailed discussion on all these topologies

**SINGLE EDGE-TRIGGERED FLIP-FLOP (SET)**

These types of flip-flops transfer the data in any of the edges of the clock, i.e. either in the positive edge or in the negative edge. The master-slave concept is applied to prepare a conventional flip-flop. The configuration is so formed that the output of the master latch becomes the input for the slave latch, again, the output received from the slave latch becomes the output of the FFs. The most conventional FF SET is proposed (Fig. 2a) [11]. Here, a transmission gate is structured, called TG1 at the master stage to get D (data output). The process largely depends on two control signals CLKB and CLK just before the clock gets the expanding edge. On the other hand, TG2, i.e. the slave side is added but remains non-conductive when TG1 is active, the vice versa is also true.

**DOUBLE EDGE-TRIGGERED FLIP-FLOP (DET)**

In this type of flip-flop, both the rising and falling edge holds the data simultaneously. Several DET FFs could be found which normally takes a good amount of signal area and also produces undesired inner switching [12] [13] [14]. The topology is good at reducing the gate density as also clock skew. A complete description of the circuit can be understood from Fig. (2b). It is made with two latches connected parallely. These are upper and lower data path. Here, the transistors MP2, MP3 MN1, and INV1 makes the upper data path and MN2, MN3, MP1, and INV2 create the lower data path. In each stage one stuff is visible on the rising edge while at the same time the other is observable on the dropping edge of the clock. Here, when the signal node XB is at its lower end, MP2 is such a transistor that is capable of providing necessary response to break the storage node X considerably to VDD. Just in the same process, when the signal node YB is visibly high, the transistor MN2 creates a response to break the Y node to GND. When data and clock both are high, the data path in the upper half becomes conducive. In this condition, the node X grabs the high local part through the transistor MP2. At the same time, in the lower data path, the previously held data is quickly transmitted as an output in the Q node that passes through MN3. When the clock is at the lower end, the lower data path starts working and the node Y uses the transistor MN2 and goes with the low logic. During this period, the upper data path promptly begins to send the previous data that was on hold with it through MP3 in Q (the output node).

**SEMI-DYNAMIC FLIP-FLOP**

In Figure 2c, we can see a block diagram SDFF (Semi-Dynamic flip-flop). We can concentrate on the evaluation and pre-charge region of operation. The circuit here is called semi-dynamic as it is made of dynamic input with static operation stage. The pre-charge phase is reached with the falling edge of the clock. To retain the earlier state, Node X gets high pre-charge. Node X also cut off Q from its input stage. At the time of pre-charge, the node S stays at a high charge in the transistor N1 because CKD is at the lower end at the same time. The flip-flop gets into the evaluation phase with the rising of the clock:

1. When D is at “0” state, X gets a higher value, at that time, Q remains low. Otherwise, Q may discharge with the help of the transistors N4 and N5 to get higher values at QB.
2. When D is at “1” state and X steadily gets into the lower value, the transistor exists till the transition is finished. During this phase, the feeble cross-coupled inverters make the flip-flop static. Now, it is possible for the last inverter to safeguard the output node.

To stop shutting off the transistor, N1 is placed in between CKD and node X.

**HYBRID LATCH FLIP-FLOP (HLFF)**

HLFF or Hybrid Latch Flip-Flop put the data at one end, at the same time, obliterates the delay or obstruction of the reverse side of the clock. HLFF is designed to reduce the load on the clock and latch latency to a large extent. Here, the fundamental operation is just like the latch. It provides an easy-going clock edge that helps in passing the load and decreasing the clock skew on the cyclical time. In Figure 2d, we can see the fundamental make of HLFF. Before the edge of the clock rises, the node Q holds the existing data while node X is pre-charged to VDD. It happens because the transistor N1 and N4 are switched off while N3, N6, and P1 are switched on at that moment. Just when the clock starts rising, N1 and N4 gets turned on while N3 and N6 wait for inverter delays related to three inverters. If the transition of CFDB is visibly low, the following activities will be visible:

1. At first, the node X is immediately decoupled from D
2. Then it may maintain that logic, or
3. It starts to pre-charge to VDD with the help of P3.

At the clock’s negative edge, the decoupled node X is fully pre-charged while it preserves the charge of X to VDD. For example, when the operating frequency is 500MHz and the design is made with the half of the clock load capacitance, it will show a latency of $\frac{2}{3}$ of the combined interruptions of the transparent low and transparent high. Hence, the net outcome is 10% improvement in cycle time and 30% reduction in the clock load.

**PULSE-TRIGGERED FLIP-FLOP (P-FF)**

Pulse-Triggered Flip-Flop or P-FF is one of the post popular master-slave FF known in this sector. In this design, two aspects are vital: a latch for data storage and a pulse generator for creating strobe signal. Two types of P-FF are found:

1. Implicit type – Here, the pulse creator is a built-in logic of the latch design. This is best adjustable for the management of the power.
2. Explicit type – Here, the pulse generator and latch designs are differentiated. This design has overcome the time management issues but not so good in width control of the pulse or diving the voluminous capacitive load when one pulse generator is shared with many other latches.

The design is depicted in Figure 2e. This design decreases the number of NMOS transistors that are used along the path of discharge. It provides necessary support to the pull-down strength that is available when the input data is “1”. Now, when the clock is at its negative edges, i.e. both CLK and D are “0”, the node z will be floating for the time being. On the other hand, the positive edge transistors N2 and N3 help to make the weak logic really high. This process can turn on the N1 transistor but some noticeable delay will be visible for the inverter I1. At this point, node X experience a rise in the voltage, transistor P3 gets turned off, and data is introduced along the width of the created pulse. The power of switching is lessened remarkably because of poor fluctuation in voltage. Here, the transistors N2 and N3 enhance the process of the creation of pulse.

**SENSE-AMPLIFIER –BASED FLIP-FLOP (SAFF)**

SAFF is proficient in taking both true and harmonized inputs and create similar types of outputs. They are manufactured from the clocked sensed amplifier which helps to get a response even when the voltage fluctuation is really small. The key problems in this flip-flop system are the slave element which is prepared by SR NAND latch [15] [16]. It suffers from the drawback that any of the internal
nodes available here can float below the normal level when the clock is at a higher level. As the circuit works with a lower number of transistors, an asymmetrical delay may occur that marks slower high to low delay in the clock to output process.

This paper interprets the high-speed flip-flop possessing sense-amplifier. This was first proposed by Antonio and his team [10]. The circuit is as shown in the Fig. 2f. Here the topology is divided into two stages:

1. Output latch stage – It is manufactured with a hybrid solution that is available through NAND and N-C2MOS.
2. Sense-amplifier stage - It is manufactured through a conventional process.

Pre-charge of the nodes Rbar and Sbar take place in the negative edge period. During the opposite phased, i.e. positive output phase, Sbar becomes zero but Rbar remain high at that period. This induces transistor N5 to switch off while P1 switches on. During that same period, the output node Qbar is locked through N3, N4, and N6.

**WRITE-PORT MASTER-SLAVE FLIP-FLOP (WPMS)**

This type of flip-flop very much resembles the master-slave construction of flip-flop. But the application of each individual latch is accomplished through SRAM 6T cell. This application is depicted in Fig 2g, as referred in [11]. The design is completed with the keeper circuit made of single NMOS each is attached to both side that is again driven by a real and harmonizing clock. The keeper is useful in performing push-pull from both sides when changing the state is necessary. In WPMS you can’t find any PMOS except the circuit of the keeper. Naturally, the delay in the clock is much reduced so also the data-path.

**TRUE SINGLE-PHASE-CLOCK FLIP-FLOP (TSPC)**

TSPC requires just one clock signal that is not overturned and rightly adjustable in both static and dynamic circuits of CMOS. Figure 2h is showing that topology with a detailed reference in [12]. The transistors N4 and P1 help to keep its previous state on the clock’s falling edge latch. On the other hand, the D inputs on the rising edge are controlled through the samples P1, N1, N3, and N4.

**CLOCKED CMOS FLIP-FLOP (C2CMOS) – A CLOCK-SKEW INSENSITIVE APPROACH**

Figure 2i shows a positive edge-triggered process that depends on the master-slave concept that is not sensitive to the clock overlay [10] [11]. This is called Clocked CMOS, abbreviated as C2CMOS. This operates in 2 phases:

- **CLK = 0**, in this condition the 1st driver gets switched on. The master stage stays in evolution mode and acts as an inverter sampler that applied the inverted form of D available in the internal node X.
- **CLK = 1**, here, the master stage remains in the hold mode. The charge already available from the previous stage is flown to the output node that acts as an inverter in the slave stage.

CONCLUSION

This paper concentrated on the most commonly used flip-flop in 0.12μm CMOS technologies. Comparisons are made with respect to power dissipation, delay, and area of the most popular designs. Different topology has different characteristics and benefits: the fastest one is C-CMOS, its area, power dissipation, and delay are lesser than any other systems in this realm, while in the matters of power consumption the best ones are TSPC, P-FF, and SAFF. On the other hand, SDFF and HLFF are considered as the best topology as far as latency and clock skew are concerned. In general, considering the influence of the layout parasitics, simple and fundamental and conventional structures are much popular and widely accepted topology in micrometer systems.
REFERENCES


