GENERATION OF PWM PULSES IN VHDL TO DRIVE THREE PHASE INVERTER

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ABSTRACT

The basic thing of the paper is to implement the drive circuit for 3 phase inverter using VLSI. Continuous Electricity is the basic need of life. Inverter serves the society in this concern. Along with Generation of power, distribution of power is equally important. It is a utility the provision of which has become synonymous with progress. In this paper, the programming language used is VHDL to generate the PWM pulses & gives it to the control circuit.

***Keywords*:** PWM, VHDL, FPGA, CPLD, VLSI

INTRODUCTION

Software-Hardware is an emerging concept in the electronics world. The scenario on the hardware technology front is changing with emergence of finer hardware manufacturing technologies. These manufacturing processes have enabled to bring out programmable hardware devices with large inbuilt functionality. The software development platforms are being made available with real time emulation testing facilities resulting in shorter design and development cycle. This has allowed the user to design and test the three phase inverter in simulated environment.

The Complex Programmable Logic Devices (CPLD) and Field Programmable Gate Arrays (FPGA) are complex hardware programmable devices. These devices have large in built programmable functionality, which allows them to be used for implementing complex digital circuits in various fields. The availability and cost of system tools along with cost of CPLD or FPGA were prohibitive factors for industrial utilization/consumption. This technology was primarily used to design ASIC (Application Specific Integrated Circuits) only. The technology explosion and decreasing costs of electronic design tools and components have brought this technology in the realm of medium and small-scale industries. It is predicted that these devices (CPLD and FPGA) will be directly used in the product manufacturing rather than manufacturing ASIC. Availability of technology and devices has opened many new avenues for digital system designers. As VLSI became possible you could build a system from by combining many standard ICs just by instantiating the required IC as a

component. VHDL (Very High Speed Integrated Circuit Hardware Description Language) is becoming default standard language for programming digital systems. Other programming languages are Verilog and Abel.

GENERATION OF PWM SIGNAL (Using VLSI):

It is to be noted that the control of the output AC voltage is been done through PWM signal which offers following advantages over the traditional methods:

1. PWM serves the Dual purpose of voltage control and harmonics reduction.
2. The PWM pulses are generated with the help of software, thus reduced effects of EMI and RFI
3. Overall cost and weight of the system is reduced by this method

This PWM signal generation is been done using state of art VLSI technology, where a HDL code is written using VHDL and it is been downloaded into a Flex10k FPGA chip. 6 output pins of the FPGA chip give the required 6 PWM pulses.

The VHDL Code is been written in behavioral style of modeling, other way structural or dataflow style of modeling can also be used. A general format of Algorithm is given in fig., which gives an idea about the VHDL code.

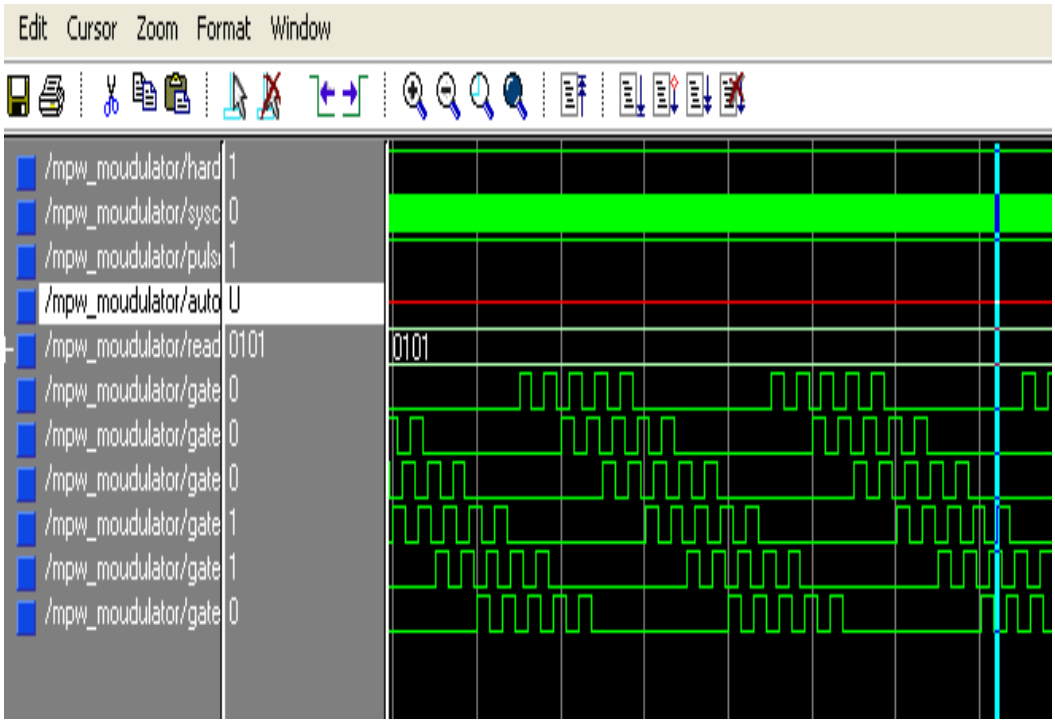

Fig.1. PWM signal Obtained after Simulation of VHDL code

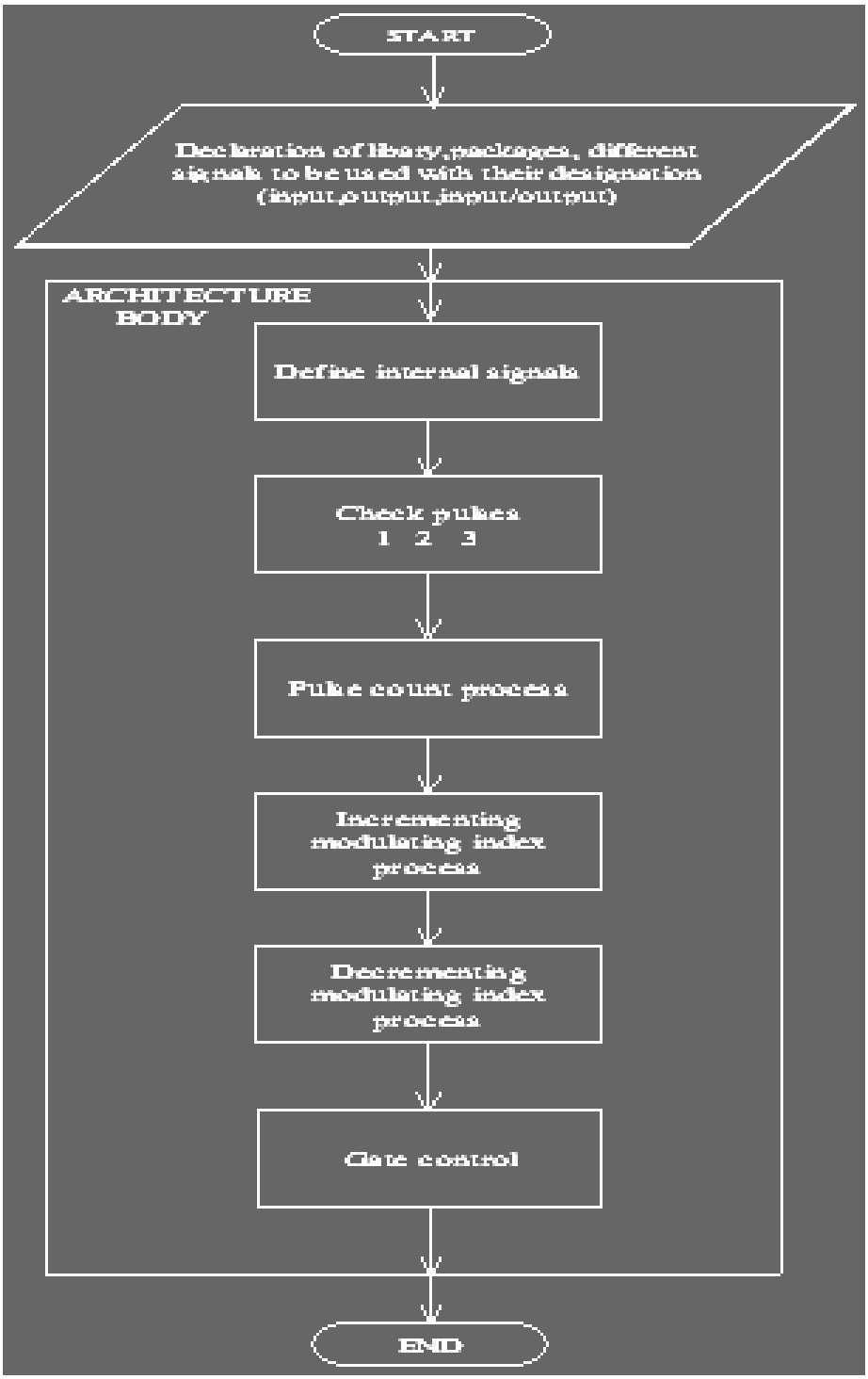

Fig.2. Algorithm of the VHDL code for generation of PWM pulses

The three phase bridge inverter

A three phase output can be obtained from a configuration of six transistors and six diodes as shown in fig. two types of control signals can be applied to the transistors: 180˚ conduction or 120˚ conduction. The 180˚ conduction has better utilization of the switches and is the preferred method and the same is used in the paper.

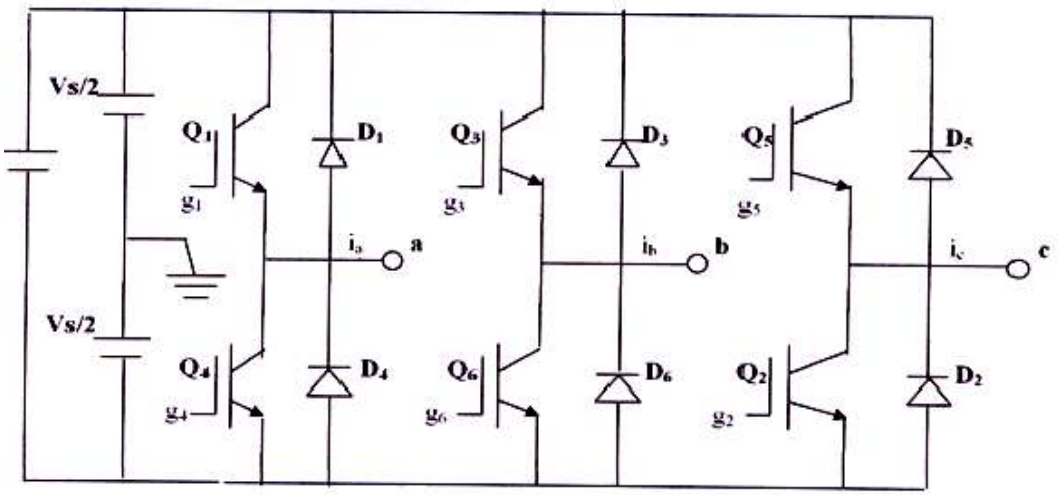

Fig.3 Three-phase bridge inverter

180-degree conduction

Each transistor conducts for 180˚. Three transistors remain on at any instant of time. When transistor $Q_1$is ON, terminal *a* is connected to the positive terminal of the dc output voltage. When transistor Q_4 is switched ON, terminal *a* is brought to the negative terminal of the dc source. There are six modes of operation in a cycle and the duration of each mode is 60^0. The transistors are numbered in the sequence of gating the transistor (e.g., 123, 234, 345, 456, 561, and 612). The gating signals shown are shifted from each other by 60^0 to obtain three-phase balanced (fundamental) voltage.

The switches of any leg of the inverter (S_1 & S_4, S_3 & S_6, S_5 & S_2) cannot be switched ON simultaneously, this would result in short circuit across the dc link voltage supply. In any mode (120˚/180˚) six pairs or triplets are possible, each conducting for a period of 60^0

CONCLUSION

Based on the results obtained, following conclusions can be drawn

1. A three phase inverter is designed using VLSI and implemented successful
2. The PWM pulses are generated using VHDL code are applied to the three phase driving circuit.

3. The three phase inverter operates in four modes.
4. The output power delivered to load can be controlled by varying the modulation index (read mode index) from 0001 to 1010.

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